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CONTINUATION APPLICATION

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TITLE: DISCRETE-TIME SAMPLING OF DATA FOR USE IN SWITCHING REGULATORS

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DISCRETE-TIME SAMPLING OF DATA FOR USE IN SWITCHING REGULATORS

BACKGROUND

The present invention relates generally to voltage regulators, and more particularly to control systems for switching voltage regulators.

Voltage regulators, such as DC to DC converters, are used to provide stable voltage sources for electronic systems. Efficient DC to DC converters are particularly needed for battery management in low power devices, such as laptop notebooks and cellular phones. Switching voltage regulators (or simply "switching regulators") are known to be an efficient type of DC to DC converter. A switching regulator generates an output voltage by converting an input DC voltage into a high frequency voltage, and filtering the high frequency input voltage to generate the output DC voltage. Specifically, the switching regulator includes a switch for alternately coupling and decoupling an unregulated input DC voltage source, such as a battery, to a load, such as an integrated circuit. An output filter, typically including an inductor and a capacitor, is coupled between the input voltage source and the load to filter the output of the switch and thus provide the output DC voltage. The switch is typically controlled by a pulse modulator, such as a pulse width modulator or a pulse frequency modulator, which controls the switch. A feedback circuit generates a control signal which controls the duty cycle of the pulse modulator in order to maintain the output voltage at a substantially uniform level.

In traditional switching regulators, the feedback controller continuously measures the output voltage and uses this measurement to continuously generate a control signal for the pulse modulator. Such a continuous feedback controller operates using analog circuits, such as resistors, capacitors and op-amps. Unfortunately, these analog circuits are expensive and/or difficult to fabricate as integrated circuits. Specifically, special techniques are needed to fabricate resistors in semiconductor devices. In addition, these analog circuits do not easily interface with any digital circuits that may be fabricated in the same semiconductor device.

SUMMARY

In one aspect, the invention is directed to a voltage regulator having an input terminal to be coupled to an input voltage source and an output terminal to be coupled to a load. The voltage regulator includes a power switch to alternately couple and decouple the input terminal to the output terminal with a variable duty cycle, a filter disposed between the input terminal and the output terminal to provide a substantially DC voltage at the output terminal, a sampling circuit to make measurements of an electrical characteristic of the voltage regulator at discrete moments of time, and a feedback circuit coupled to the sampling circuit and the power switch, the feedback circuit configured to use the measurements to control the duty cycle to maintain the DC voltage substantially constant.

Implementations of the invention may include the following. The electrical characteristic may be a voltage at the output terminal or a current passing through the filter. The sampling circuit may include a capacitor, a first sampling switch connecting the capacitor to the output terminal, and a second sampling switch connecting the capacitor to the feedback circuit, so that the measurement is made when the first sampling switch opens, is stored as a charge in the capacitor, and is provided to the feedback circuit when the second sampling switch closes. Alternately, the sampling circuit may include a capacitor, a first sampling switch connecting a first plate of the capacitor to a first terminal of the power switch, a second sampling switch connecting a second plate of the capacitor to a second terminal of the power switch, and a third sampling switch connecting the capacitor to the feedback circuit, so that the measurement is made when the first and second sampling switches open, is stored as a charge in the capacitor, and is provided to the feedback circuit when the third sampling switch closes. The sampling circuit may make the measurement just prior to the power switch opening and/or closing. The sampling circuit may make a first measurement of the electrical characteristic when the power switch is closed and make a second measurement of the electrical characteristic when the power switch is open. The feedback circuit may use an average of the first and second measurements to control the duty cycle. The sampling circuitry may include a capacitor, a first sampling switch connecting the capacitor to an electrical path between the input terminal and the output terminal, and a second sampling switch connecting the capacitor to the feedback circuit. The second sampling switch may be

configured to close when the first sampling switch open, and the first sampling switch may be configured to open just before the power switch opens and/or closes. The power switch may be driven by a switching voltage waveform and the sampling switches may be driven by a sampling voltage waveform, and the voltage regulator may further include a timing circuit to delay the switching voltage waveform relative to the sampling voltage waveform, e.g., by approximately the time constant delay of the sampling circuit. The feedback circuit may generate a control signal, and the voltage regulator may further include a pulse modulator connected to the feedback circuit and the power switch to set the duty cycle in response to the control signal. The feedback circuit may include one or more switched-capacitor circuits coupled to the sampling circuit to convert the measurement into a charge and to generate the control signal from the charge. The sampling circuit may include an analog-to-digital converter (ADC) coupled to the sampling circuit to convert the measurement into a digital signal, and a processor coupled to the ADC to generate the control signal from the digital signal. The power switch may include a first switch connecting the input terminal to an intermediate terminal and a rectifier, such as a second switch, connecting the intermediate terminal to ground, and the output filter may be connected between the intermediate terminal and the output terminal.

In another aspect, the invention is directed to a voltage regulator having an input terminal to be coupled to an input voltage source and an output terminal to be coupled to a load. The voltage regulator includes a power switch to alternately couple and decouple the input terminal to the output terminal with a variable duty cycle, a filter disposed between the switch and the output terminal to provide a substantially DC voltage at the output terminal, a sampling circuit to make a measurement of a current passing through the output filter, and a feedback circuit connected to the sampling terminal and the power switch configured to use the measurement to control the duty cycle to maintain the DC voltage at a substantially constant level. The sampling circuit includes a capacitor, a first sampling switch connecting a first plate of the capacitor to a first terminal of the power switch, a second sampling switch connecting a second plate of the capacitor to a second terminal of the power switch, and a third sampling switch connecting the capacitor to a sampling terminal.

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Advantages of the invention may include the following. The feedback controller of the voltage regulator uses a discrete-time data sampling system to control the pulse modulator. Such a feedback controller may be implemented using digital and/or switched-capacitor based circuitry, and may be fabricated using known processes suitable for complimentary metal oxide semiconductor (CMOS) fabrication techniques. This reduces the number of discrete (off-chip) components in the controller. The invention permits the feedback controller to be implemented using an analog-to-digital converter and a micro-processor so that the duty cycle of the switch may be controlled by a software-implemented algorithm. In addition, the use of digital designs and traditional CMOS fabrication techniques permit the voltage regulator to be constructed more cheaply. Furthermore, the discrete times at which the voltage and current are sampled may be selected to provide a high accuracy and a minimum amount of switching noise.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a switching regulator in accordance with the present invention.

Figure 2 is a schematic circuit diagram of one embodiment of the switching regulator of Figure 1.

Figure 3 is a timing diagram showing the switching voltage from the pulse modulator of the switching regulator of Figure 2.

Figure 4 is a timing diagram showing the intermediate voltage at the intermediate terminal of the switching regulator of Figure 2.

Figure 5 is a timing diagram showing the output voltage at the output terminal of the switching regulator of Figure 2.

Figure 6 is a timing diagram showing the current through the output filter of the switching regulator of Figure 2.

Figure 7 is a timing diagram showing the sampling voltage to drive the sampling circuits of the switching regulator of FIG. 2

Figure 8 is a schematic circuit diagram showing a discrete-time current-sampler from the feedback controller of the switching regulator of Figure 2.

Figure 9 is a schematic diagram showing a feedback control signal generator from the

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feedback controller of the switching regulator of Figure 2.

Figure 10 is a timing diagram of the ramp voltage and control voltage input to the pulse modulator of the switching regulator of Figure 2.

Figure 11A and 11B are schematic circuit diagrams showing alternate embodiments of the discrete-time voltage sampler.

Figure 12 is a schematic diagram of an alternate embodiment of a feedback controller.

Figure 13 is a schematic diagram of an another alternate embodiment of a feedback controller.

Figure 14 is a schematic diagram of another embodiment of the switching regulator of Figure 1.

DETAILED DESCRIPTION

Referring to Figure 1, a switching regulator 10 is coupled to an unregulated DC input voltage source 12, such as a battery, by an input terminal 20. The switching regulator 10 is also coupled to a load 14, such as an integrated circuit, by an output terminal 24. The switching regulator 10 serves as a DC-to-DC converter between the input terminal 20 and the output terminal 24. The switching regulator 10 includes a switching circuit 16 which serves as a power switch for alternately coupling and decoupling the input terminal 20 to an intermediate terminal 22. The switching circuit 16 includes a rectifier, such as a switch or diode, coupling the intermediate terminal 22 to ground. The switching regulator also includes a pulse modulator 18 for controlling the operation of the switching circuit 16. The pulse modulator 18 causes the switching circuit 16 to generate an intermediate voltage having a rectangular waveform at the intermediate terminal 22. Although the pulse modulator 18 and the switching circuit 16 will be illustrated and described below as a pulse width modulator, the invention is also applicable to various pulse frequency modulation schemes.

The intermediate terminal 22 is coupled to the output terminal 24 by an output filter 26. The output filter 26 converts the rectangular waveform of the intermediate voltage at the intermediate terminal 22 into a substantially DC output voltage at the output terminal 24. Although the switching circuit 16 and the output filter 26 will be illustrated and described below for a buck converter topology, the invention is also applicable to other voltage regulator

topologies, such as a boost converter or a buck-boost converter topology.

The output voltage is regulated, or maintained at a substantially constant level, by a feedback circuit 28. The feedback circuit 28 includes sampling circuitry 30 which measures the output voltage and the current passing through the output terminal 24 at discrete times during each cycle of the switching circuit 16. The measured voltage and current are input to a feedback control signal generator 32. The feedback control signal generator 32, in turn, generates a control voltage on a duty cycle control line 34 to control the pulse modulator 18. The sampling circuitry 30 and the feedback control signal generator 32 may be constructed utilizing entirely digital and switched-capacitor based components. Thus, most of the switching regulator 10, including the switching circuit 16, the pulse modulator 18, and the feedback circuit 28, may be implemented or fabricated on a single chip utilizing conventional CMOS techniques. Each of the elements in the switching regulator 10, i.e., the switching circuit 16, the pulse modulator 18, the output filter 26, the sampling circuitry 30, and the feedback control signal generator 32, will be discussed in greater detail below.

Referring to Figure 2, the switching circuit 16 and the output filter 26 are configured in a buck converter topology. Specifically, the switching circuit 16 includes a switch, such as a first transistor 40 having a source connected to the input terminal 20 and a drain connected to the intermediate terminal 22, and a rectifier, such as a second transistor 42 having a source connected to ground and a drain connected to the intermediate terminal 22. The first transistor 40 may be a P-type MOS (PMOS) device, whereas the second transistor 42 may be an N-type MOS (NMOS) device. Alternately, the second transistor 42 may be replaced or supplemented by a diode to provide rectification. Also, both transistors may be NMOS devices. The first and second transistors 40 and 42 may be driven by a switching voltage V_s on switching lines 48a and 48b.

Referring to Figure 3, the pulse modulator generates a switching voltage V_s having a rectangular waveform. The switching voltage V_S has a frequency, F_S, of $1/T_S$ and a variable duty cycle, d, which is controlled by the feedback control signal generator. The duty cycle d is percentage of each period T_S that the switching voltage is on, i.e., low. The frequency F_S of the switching voltage may be in the range of about ten kilohertz to several megahertz. When the switching voltage V_S is low, the first transistor is closed and the second transistor is open (PMOS

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conduction period 50), whereas if the switching voltage V_S is high, the first transistor is open and the second transistor is closed (NMOS conduction period 52). Thus, during the PMOS conduction period 50, the intermediate terminal is connected to the input terminal, whereas during the NMOS conduction period 52, the intermediate terminal is connected to ground. Although not illustrated, the switching voltages on the switching lines 48a and 48b may be triggered by conventional techniques so that the PMOS and NMOS conduction periods 50 and 52 are separated by a dead time to ensure that both switches are not open simultaneously.

Referring to Figure 4, the resulting intermediate voltage V_X at the intermediate terminal is a rectangular waveform having a variable duty cycle d (the percentage of the cycle in which the intermediate terminal is connected to the input terminal) and a constant frequency F_s.

Returning to Figure 2, the intermediate voltage V_x is filtered by the output filter 26 to generate an output voltage V_{out} at the output terminal 24. The output filter 26 includes an inductor 44 connected between the intermediate terminal 22 and the output terminal 24 and a capacitor 46 connected in parallel with the load 14. During the PMOS conduction period, the voltage source 12 supplies energy to the load 14 and the inductor 44 via the first transistor 40. On the other hand, during the NMOS conduction period, the energy is supplied by the inductor 44. The resulting output voltage V_{out} is a substantially DC voltage. The average voltage V_0 of the output voltage V_{out} is given by the product of the input voltage V_{in} and the duty cycle d, i.e., $V_o = d \times V_{in}$. The average output current I_o passing through the output terminal 24 is given by the average voltage V_o divided by the effective resistance R_o of the load, i.e., $I_o = V_o/R_o$.

Unfortunately, the actual output voltage V_{out} is not exactly equal to the average voltage V_0. Referring to Figure 6, the output voltage V_{out} will include a ripple ΔV which is given by the following equation:

$$\Delta V \approx \frac{V_0 \cdot (1-d)}{8 \cdot L_f \cdot C_f \cdot f_s^2}$$

where d is the duty ratio, L_f is the inductance of the inductor 44, C_f is the capacitance of the capacitor 46, and f_s is the switching frequency.

Similarly, the actual output current I_{out} is not exactly equal to the average current I_o.

Referring to Figure 6, the output current I_{out} will be a triangular waveform with a period T_s and a peak-to-peak ripple ΔI which has its maximum and minimum peaks equidistant from the average load current I_0. The peak-to-peak ripple ΔI is given by the following equation:

$$\Delta I = \frac{V_0 \cdot (1-d)}{L_f f_s}$$

where d is the duty cycle, L_f is the inductance of the inductor 44, and f_s is the switching frequency.

As previously discussed, the switching regulator includes sampling circuitry to measure the output voltage V_{out} and the output current I_{out}. The sampling circuitry measures the output voltage at one or more discrete times during each cycle of the switching circuit. The sampling circuitry also measures the output current at one or more discrete times during each cycle of the switching circuit. However, since the output current cannot be measured directly, the sampling circuitry may actually measure a voltage difference which is representative of output current. Nevertheless, some of the description which follows is phrased as if the current were measured directly.

The feedback control signal generator uses the measured voltages and currents to determine the average output voltage V_0 and average output current I_0. The average output voltage V_0 and average output current I_0 are used to control the duty cycle of the power switch. It should be noted that the feedback circuit may use the voltage and current measurements to control the power switch without the intermediate step of determining the average values. Some of the description which follows is phrased as if the average values are calculated and provided as separate signals, although, as noted, this is not necessarily the case.

Referring to Figures 4, 5 and 6, the maximum output current I_{out} is reached at the end of the PMOS conduction period 50 and the minimum output current I_{out} is reached at the end of the NMOS conduction period 52. In addition, the output voltage V_{out} passes through its average value at the end of the PMOS and NMOS conduction periods 50 and 52. Therefore, in order to estimate the average output voltage V_0, a first voltage measurement V_1 is made at the end of the PMOS conduction period 50, a second voltage measurement V_2 of the output voltage is made at the end of the NMOS conduction period 52, and the two measurements are averaged. Similarly,

to estimate the average output current I_o, a first representative measurement V_{I1} of the current I_1 is made at the end of the PMOS conduction period 50, a second current measurement V_{I2} representative of the current I_2 is made at the end of the NMOS conduction period 52, and the two measurements are averaged. Because switching noise occurs when the transistors are switched on or off, if the measurements are made just before the switching voltage V_s changes, there is a minimum amount of switching noise in the average current and voltage.

Returning to Figure 2, a significantly simplified voltage sampler is shown. Current sampling is not shown explicitly in Figure 2; it will be explained with reference to Figure 8. The sampling circuitry 30 includes two voltage sampling capacitors 60a and 60b that are connected to the output terminal 24 by two voltage sampling switches 62a and 62b, respectively. The voltage sampling capacitors 60a and 60b may be connected by additional sampling switches 64a and 64b to the feedback control signal generator 32 via voltage sampling terminals 58a and 58b. The sampling switches may be configured so that switches 64a and 62b are closed when switches 62a and 62b are open, and vice-versa. While switch 62a is closed and switch 64a is open, current flows from the output terminal 24 into voltage sampling capacitor 60a. However, when switch 62a is opened and switch 64b is closed, the output voltage stored in voltage sampling capacitor 60a in the form of a charge is transferred onto voltage sampling terminal 58a to provide the first voltage measurement V_1. Similarly, while switch 62b is closed and switch 64b is open, current flows into voltage sampling capacitor 60b, but when switch 62b is opened and switch 64b is closed, the output voltage stored in voltage sampling capacitor 60b is transferred onto voltage sampling terminal 58b to provide the second voltage measurement V_2. Sampling switches 62a, 62b, 64a and 64b are driven by a sampling voltage V_{sample} on sampling control lines 66a and 66b.

Referring to Figure 7, the sampling voltage waveform V_{sample} switches between high and low states just before the end of the PMOS conduction cycle and the NMOS conduction cycle. Although not shown explicitly, the sampling voltage on control lines 66a and 66b may be offset so that switches 62a, 62b and 64a, 64b are not open simultaneously.

Returning to Figure 2, the switching lines 48a and 48b and the sampling control lines 66a and 66b may be connected to a timing circuit 68. The timing circuit 68 delays the switching voltage waveform V_s relative to the sampling voltage waveform V_{sample} to ensure that sampling

occurs just before the transistors 40 and 42 flip in order to minimize noise. Thus, voltage sampling terminal 58a provides the first voltage V_1 measured at the end of the PMOS conduction period, and voltage sampling terminal 58b provides the second voltage V_2 measured at the end of the NMOS conduction period. The sampling voltage waveform V_{sample} may be offset from the switching voltage waveform V_s by a delay T_D which is approximately equal to the time constant delay of the sampling circuit, i.e., about the time required by the sampling circuitry 30 to take the voltage and current measurements. The delay T_D may be on the order of several nanoseconds. Preferably, the delay T_D is larger than the time required to sample voltage and current.

As previously mentioned, sampling circuitry 30 also measures the output current I_{out} at the end of the PMOS conduction period and the end of the NMOS conduction period. The current passing through the output terminal 24 is equal to the inductor current I_{LF} passing through the inductor 44. However, the inductor current I_{LF} cannot be measured directly; it must be inferred from a voltage measurement taken across a resistive element through which the current passes.

The sampling circuitry 30 includes a current sampler, one implementation of which is shown in Figure 8. In this implementation, the current sampler uses the first and second transistors 40 and 42 as the resistive elements for the measurement of the inductor or output current. For each transistor 40 and 42, the sampling circuitry includes four current sampling switches 70, 72, 74 and 76, and a current sampling capacitor 78. The top plate of the current sampling capacitor 78 is connected to the source of the transistor (i.e., the input terminal 24 for the first transistor 40 and ground for the second transistor 42) by the first current sampling switch 70. Similarly, the bottom plate of the current sampling capacitor 78 is connected to the drain of the transistor (i.e., the intermediate terminal 22 for both the first and second transistors 40 and 42) by the second current sampling switch 72. The top plate of the current sampling capacitor 78 is coupled to a current sampling terminal 80 by the third current sampling switch 74, and the bottom plate of the current sampling capacitor 78 is connected to a reference voltage V_{REF} by the fourth current sampling switch 76. The first and second switches 70 and 72 open simultaneously at the end of the conductive period of the transistor to which they are attached or

connected, whereas the third and fourth switches 74 and 76 close when the first and second switches 70 and 72 open. The control signals to activate the switches 70, 72, 74 and 76 may be generated on timing lines 82a and 82b by the timing circuit 68 in a manner similar to the control signals for the sampling switches. Thus, at the end of the conduction period to which the current sampler is connected, a voltage representing the inductor current is supplied to the current sampling terminal 80. Two current sampling circuits provide the voltage measurements V_{I1} and V_{I2} which are representative of the currents I_1 and I_2, respectively.

The voltage and current measurements may be made at a variety of discrete times. For example, a single current measurement could be made at the middle of the NMOS conduction period. However, by sampling the voltage and current just prior to the end of the conduction periods of the first transistor 40 and the second transistor 42, the sampled signals provide the best estimate for the average values of the inductor current and capacitor voltage and are taken when the switching noise is at a minimum.

Referring to Figure 9, the sampled data V_1, V_2, V_{I1}, and V_{I2} on sampling terminals 58a, 58b, 80a, and 80b are supplied to the feedback control signal generator 32. The feedback control signal generator uses these signals to generate a control voltage $V_{control}$ on the duty cycle control line 34. This control voltage is used by the pulse generator 18 to modulate the duty cycle of the switching circuit 16 to maintain the average voltage V_o at the output terminal at a substantially constant level. V_o andand 172a and

The feedback control signal generator can determine $V_{control}$ according to various algorithms. For example, sampling terminals 58a, 58b and 80a, 80b may be connected to switch capacitor circuits 170a and 170b, respectively, to effectively combine and average the sampled voltages V_1, V_2 and V_{I1} ,V_{I2} to generate the average values V_o and V_{I0}, respectively. The averaged value V_{I0} is scaled by a constant K_I by amplifier 172b respectively. The averaged voltage V_o is compared to a reference voltage V_{ref} by a first summing circuit 174. The difference between the averaged voltage V_o and the reference voltage V_{ref} is is scaled by a constant K_V by amplifier 172a. In addition, the difference between the averaged voltage V_o and the reference voltage V_{ref} is integrated by an integrator 176 to generate an integrated voltage V_{int}. Finally, the three inputs $K_V V_0$, $K_I I_0$ and V_{int} are combined by a second summing circuit 178 to generate the

control signal $V_{control}$.

Returning to Figure 2, a significantly simplified pulse modulator 18 is shown. The pulse modulator 18 converts the control voltage $V_{control}$ on the duty cycle control line 34 into a timing voltage waveform on a timing line 104. The pulse modulator 18 includes a ramp generator 100 and a comparator 102. Referring to Figure 10, the output of the ramp generator is a saw tooth wave having a frequency of $1/T_s$, a minimal voltage of V_{min} and a maximum voltage of V_{max}. The comparator compares the control voltage $V_{control}$ to the ramp voltage V_{ramp} and outputs a high voltage on the timing line if $V_{control}$ is greater than V_{ramp}, and a low voltage on the timing line if $V_{control}$ is less than V_{ramp}. Returning to Figure 2, the timing voltage waveform on the timing line 104 is sent to the timing circuit 68. The timing circuit 68 may output the timing voltage waveform sampling voltage V_{sample} on the sampling control lines 66a and 66b. The timing circuit 68 may generate a switching voltage V_s on the switching lines 48a and 48b which is offset from the sampling voltage waveform V_{sample} by a small delay T_D. Thus, the sampling switches (e.g., switches 62a, 62b, 64a and 64b) are triggered slightly before the transistors 40 and 42 in the switching circuit 16.

If $V_{control}$ increases, the duty cycle D of switching voltage V_s decreases. On the other hand, if control voltage $V_{control}$ decreases, duty cycle D increases. Therefore, the feedback circuit 28 is able to measure the output voltage V_{out} and inductor current I_{LF} at discrete times, use this data to calculate the average voltage V_0 and the average current I_0, and use the average current and voltage to modulate the duty cycle of switching voltage V_s to ensure that the output voltage remains substantially constant. Since all of the components of the feedback controller may be designed using switches and capacitors, most of the switching regulator may be fabricated utilizing conventional CMOS techniques. In addition, because the voltage and current are sampled at discrete times, the system is more compatible with conventional digital designs such as digital timing circuits.

Referring to Figure 11A, in another embodiment, a voltage sampling capacitor 60' is connected to a reference voltage V_{REF} rather than to ground. This reduces the amount of charge stored on the capacitor.

Referring to Figure 11B, in another embodiment, sampling circuitry 30" is constructed with a bottom plate sampling topology. The bottom plate of a voltage sampling capacitor 60" is

connected to the output terminal 24 by a first sampling switch 112 and to a reference voltage V_{ref} by a second sampling switch 114. The top plate of the voltage sampling capacitor 60" is connected to the same reference voltage V_{ref} by a third sampling switch 116 and to a voltage sampling terminal 58" by a fourth sampling switch 118. The first switch 112 and the third switch 116 are closed during the conduction period before the voltage measurement, whereas the second switch 114 and the fourth switch 118 are open during the conduction period before the voltage measurement. Bottom plate sampling reduces the sampling error caused by parasitic capacitance and charge injection from the switches.

One possible implementation of the feedback circuitry 28', including sampling circuitry and a feedback control signal generator, is shown in Figure 12. The feedback circuitry 28' includes voltage sampling cells 130 to measure the output voltages V_{out}, current sampling cells 132 to measure a voltage V_{DS} which represents the current passing through the inductor, and an integrator 134 which is associated with voltage sampling cells 136 to generate an integral of the difference between the difference between the measured and desired output voltage. The voltages from the voltage sampling cells 130, the current sampling cells 132, the integrator 134, and a ramp generator 138, are combined by a main summing amplifier 140. The output of the main summing amplifier 140 is sent to a comparator 142 which generates the sampling voltage. The elements in the feedback circuitry are driven by a timing signal generator 144 which generators the following signals: nmos_on/phi_nmos is high when the NMOS transistor is on; pmos_on/phi_pmos is high when the PMOS transistor is on; not_pmos_on is high when the PMOS transistor is off; nmos_even is high every other time the NMOS transistor is on; and nmos_odd is high every other time the NMOS transistor is on, but is in quadrature with the nmos_even signal. All of these signals switch low just before the gate drive buffers for their respective transistors begin switching. The voltage sampling cells include two sample cells for measuring the voltage at the end of the NMOS conduction period. One sampling cell is connected to the main summing amplifier while the other sampling cell is sampling. Thus, the main summing amplifier can use the NMOS sample take in the previous period to calculate the duty cycle to be used in the current period. Although the switchs are illustrated as JFET transisitors, they may be implemented as NMOS and PMOS transistors.

In brief, the feedback circuitry 28' calculates the duty cycle according to the following equation:

$$DutyCycle = \frac{f}{2I_{PWM}}\left(C_V(V_{ERROR}^{PMOS}+V_{ERROR}^{NMOS})+(C_{PMOS}V_{DS}^{PMOS}+C_{NMOS}V_{DS}^{NMOS})+C_I\frac{C_S}{C_F}\sum_{0}^{N}(V_{ERROR}^{PMOS}+V_{ERROR}^{NMOS})\right)$$

where f is the sampling frequency, I_{PWM} is the current from each side of the ramp generator, CV is the capacitance of the voltage sampling capacitor (e.g., 2.8 pF), C_{PMOS} is the capacitance of the current sampling capacitor for the PMOS transistor (e.g., 4 pF), C_{NMOS} is the capacitance of the current sampling capacitor for the NMOS transistor (e.g., 8 pF), C_I is the capacitance of the output sampling capacitor in the integrator (e.g., 0.8 pF), C_S is the capacitance of the sampling capacitor (e.g., 1 pF), C_F is the capacitance of the integrating capacitor (e.g., 3.5 pF), V_{DS}^{PMOS} is the voltage measurement which is representative of the output current during the PMOS conduction period, V_{ERROR}^{PMOS} is the output voltage measurement during the PMOS conduction period, V_{ERROR}^{NMOS} is the output voltage measurement during the NMOS conduction period, and V_{DS}^{NMOS} is the voltage measurement which is representative of the ouput current during the NMOS conduction period.

Referring to Figure 13, in another embodiment, the analog components of the feedback control signal generator 32 are replaced with a microprocessor 120. Specifically, sampling terminals 58a, 58b, 80a and 80b are each connected to an analog-to-digital converter (ADC) 122 to convert the sampled voltage or current into a digital signal which is sent to the microprocessor 120. The microprocessor 120 may be a combination of hardware, software, and firmware. The microprocessor 120 calculates a duty cycle signal which is converted by a digital-to-analog converter (DAC) 124 into a control voltage $V_{control}$. The microprocessor 120 may be programmed to calculate the average voltage V_0 and the average current V_{I0} from the sampled measurements V_1, V_2, V_{I1} and V_{I2}. Then, the microprocessor 120 may calculate a new control voltage from the average voltage V_0 and average current V_{I0}. For example, the microprocessor may store a control voltage used from the previous cycle, V_{old}, and calculate a new control voltage V_{new} according to a preset equation.

Referring to Figure 14, in another embodiment, the signal control generator and pulse

modulator functions are combined and implemented directly by the microprocessor 120'. The microprocessor 120' is connected directly to switching line 48. The microprocessor may be configured to calculate a duty cycle from the average voltage V_0 and average current I_0.

What is claimed is:

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